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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,677	02/18/2004	Dae-Seung Jeong	9862-000017/US	8542

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EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,677	JEONG ET AL.	
	Examiner	Art Unit	
	KABIR A. TIMORY	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-23* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 12/09/2008. Claims 1-23 are pending in this application and have been considered below.

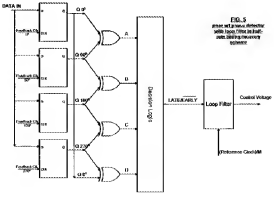
2. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 8-9, 14-17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocaman et al. (US 20040030513) in view of Laturell et al. (US 20040096013).



Regarding claims 1, 14, 16, and 21:

As shown in figure 1-24, Kocaman et al. discloses a quarter-rate phase detector comprising:

- an error circuit **(see four X-OR gates in figure 5)** to combine corresponding ones of the latched signals respectively **(see the latched signals of the four latches in figure 5)**, resulting in a plurality of intermediate signals **(A-D signals output from X-OR gate in figure 5)**; and
- a multiplexing unit **(decision logic in figure 5)** to selectively output the intermediate signals as a phase error signal **(late/early signal at the output of decision logic unit in figure 5)**.

Kocaman et al. discloses all of the subject matter as described above and four latches except for specifically teaching four latches controllable to latch, at different times according to quadrature clock signals respectively, data received by the quarter-rate phase detector so as to form latched signals.

However, Laturell et al. in the same field of endeavor, teaches four latches controllable **(figure 3 clearly shows that the 4 latches 314, 316, 318, and 320 are controllable by the I and Q (quadrature) clock signal)** to latch **(314, 316, 318, and 320 in figure 3)**, at different times according to quadrature clock signals **(CLK2I, CLK2Q, CLK2IB, AND CLK2QB in figure 3)** respectively, data received **(112 in figures 2 and 3)** by the quarter-rate phase detector **(par 0002, lines 1-5)** so as to form latched signals **(OD1-OD4 in figure 3) (par 0026, lines 7-16, par 0033, lines 1-5, par 0040-par 0048)**. Therefore, it would have been obvious to one ordinary skill in the art at

the time the invention was made to use a quarature phase detector which contains four latches as taught by Laturell et al. to modify the system and method of Kocaman et al. in order to optimize the clock recovery circuitry by centering the latch function over the time of highest signal level, thereby maximizing signal-to-noise ratio (see par 0008).

Regarding claim 2:

Kocaman et al. discloses all of the subject matter as described above except for specifically teaching wherein:

- the quadrature clock signals include signals I, Q, Ib and Qb;
- a first one of the latches is controlled by I;
- a second one of the latches is controlled by Q;
- a third one of the latches controlled by Ib; and
- a fourth one of the latches is controlled by Qb.

However, Laturell et al. in the same field of endeavor, teaches wherein:

- the quadrature clock signals include signals I, Q, Ib and Qb **(see figure 3)**;
- a first one of the latches is controlled by **I (see the clock signal for 320 in figure 3)**;
- a second one of the latches is controlled by Q **(see the clock signal for 314 in figure 3)**;
- a third one of the latches controlled by Ib **(see the clock signal for 316 in figure 3)**; and
- a fourth one of the latches is controlled by Qb **(see the clock signal for 318 in figure 3)**.

Although, the order of the four quadrature signals are different, it would have been obvious to one ordinary skill in the art at the time the invention was made to rearrange the order of the clock signal for the four latches as taught by Laturell et al. to modify the system and method of Kocaman et al. in order to optimize the clock recovery circuitry by centering the latch function over the time of highest signal level, thereby maximizing signal-to-noise ratio (see par 0008).

Regarding claim 4:

Kocaman et al. further discloses wherein the multiplexing unit is controllable to truncate the intermediate signals **(A-D signals output from X-OR gate in figure 5)**.

Regarding claim 5:

Kocaman et al. further discloses wherein the multiplexing unit is operable to form the phase error signal by cycling through the truncated intermediate signals **(A-D signals output from X-OR gate and late/early signal in figure 5)**.

Regarding claim 8:

Kocaman et al. further discloses wherein

- the corresponding latched signals are pairs of latched signals **(Q0-Q270 degrees signals output from latches in figure 5)**; and
- each pair has a first set and a second set **(see figure 5)**, the second set representing the latched signals subsequently closest in time to the first set, respectively **(see figure 6)**.

Regarding claim 9:

Kocaman et al. further discloses wherein the error circuit includes four exclusive OR (XOR) gates **(see the XOR gates in figure 5)**, each XOR gate receiving one of the pairs, respectively **(see figure 5)**.

Regarding claim 15:

Kocaman et al. discloses all of the subject matter as described above except for specifically teaching the error-signal-generating circuit is operable upon the four latched signals and is controlled by the quadrature clocks signals.

However, Laturell et al. in the same field of endeavor, teaches the error-signal-generating circuit is operable upon the four latched signals **(OD1-OD4 in figure 3)** and is controlled by the quadrature clocks signals **(CLK2I, CLK2Q, CLK2IB, AND CLK2QB in figure 3) (par 0026, lines 7-16, par 0033, lines 1-5, par 0040-par 0048)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Laturell et al. to modify the system and method of Izzard et al. in order to optimize the clock recovery circuitry by centering the latch function over the time of highest signal level, thereby maximizing signal-to-noise ratio (see par 0008).

Regarding claim 17:

Kocaman et al. discloses all of the subject matter as described above except for specifically teaching four data latches, each latch receiving the same input data, the latches being clocked by quadrature clock signals, respectively, so as to produce quadrature latched data signals.

However, Laturell et al. in the same field of endeavor, teaches four data latches **(314, 316, 318, and 320 in figure 3)**, each latch receiving the same input data **(112 in figure 3)**, the latches being clocked by quadrature clock signals **(CLK2I, CLK2Q, CLK2IB, AND CLK2QB in figure 3)**, respectively, so as to produce quadrature latched data signals **(OD1-OD4 in figure 3) (par 0026, lines 7-16, par 0033, lines 1-5, par 0040-par 0048)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Laturell et al. to modify the system and method of Izzard et al. in order to optimize the clock recovery circuitry by centering the latch function over the time of highest signal level, thereby maximizing signal-to-noise ratio (see par 0008).

5. Claims 3, 6, 7, 13, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocaman et al. in view of Laturell et al. as applied to claim 1 above and further in view of Izzard et al. (US 5,506,874).

Regarding claim 3:

Kocaman et al. and Laturell et al. discloses all of the subject matter as described above except for specifically teaching wherein the multiplexing unit is controllable by the quadrature clock signals.

However Izzard et al. in the same field of endeavor teaches wherein the multiplexing unit is controllable by the quadrature clock signals **(24 in figure 9)**.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide quadrature for the multiplexer as taught by Izzard et al. to modify the system and method of Kocaman et al. in order to control the operation of the multiplex by the quadrature signal (see figures 6 and 9).

Regarding claims 6 and 22:

Kocaman et al. discloses all of the subject matter as described above except for specifically teaching wherein the quadrature clock signals include signals I and Q; and the multiplexing unit is controlled according to the signals I and Q, respectively.

However Laturell et al. in the same field of endeavor teaches wherein the quadrature clock signals include signals I and Q **(see figure 3)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use the quarature signals as taught by Laturell et al. to modify the system and method of Kocaman et al. in order to provide I and Q clock signal for the phase detector (see figure 3).

Kocaman et al. and Laturell et al. disclose all of the subject matter as described above except for specifically teaching the multiplexing unit is controlled according to the signals I and Q, respectively.

However Izzard et al. in the same field of endeavor teaches the multiplexing unit is controlled according to the signals I and Q, respectively **(figure 1, MI' and MI", column 3, lines 5-19)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide quadrature for the multiplexer as

taught by Izzard et al. to modify the system and method of Kocaman et al. in order to control the operation of the multiplex by the quadrature signal (see figures 6 and 9).

Regarding claim 7:

Kocaman et al. and Laturell et al. disclose all of the subject matter as described above except for specifically teaching wherein the multiplexing unit includes: a first multiplexer and a second multiplexer to receive the intermediate signals, respectively; and a third multiplexer to multiplex outputs of the first and second multiplexers.

However Izzard et al. in the same field of endeavor teaches wherein the multiplexing unit includes: a first multiplexer and a second multiplexer to receive the intermediate signals, respectively **(28, 32 in figure 9)**; and a third multiplexer to multiplex outputs of the first and second multiplexers **(24 in figure 9)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made use the multiplexers as taught by Izzard et al. to modify the system and method of Kocaman et al. in order to select and generate phase error signal for the system (see figures 1, 6, and 9).

Regarding claims 13 and 23:

Kocaman et al. and Laturell et al. disclose all of the subject matter as described above except for specifically teaching wherein the rate of the intermediate signals is 1/4 of the received data rate.

However Izzard et al. in the same field of endeavor teaches wherein the rate of the intermediate signals is 1/4 of the received data rate **(column 5, lines 31-32)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the

invention was made use the quadrature phase detector as taught by Izzard et al. to modify the system and method of Kocaman et al. in order to the desired data rate (1/4) for the system (column 5, lines 31-32).

6. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izzard et al. in view of Savoj et al. (US 6,847,789).

Regarding claim 18:

As shown in figure 11, Izzard et al discloses a clock and data recovery (CDR) circuit comprising:

- a phase-error generating circuit to determine quarter-rate phase detector **(figure 11, 10, column 2, lines 43-45)**;
- a filter **(36 in figure 11)**; and
- a quadrature voltage-controlled oscillator (VCO) **(38 in figure 11)** operable upon an output of the filter **(36 in figure 11)**;
- the phase-detector **(10 in figure 11)** being controllable by the output of the VCO **(38 in figure 11) (In figure 11 shows that phase detector 10 is being controlled by the output of VCO 38)**.

Izzard et al discloses all of the subject matter as described above except for specifically teaching a charge pump operable upon an output of the phase detector and a filter operable upon an output of the charge pump.

However Savoj et al. in the same field of endeavor, teaches a charge pump **(220 in figure 2)** operable upon an output of the phase detector **(210 in figure 2)** and a filter **(230 in figure 2)** operable upon an output of the charge pump **(220 in figure 2)**.

One of ordinary skill in the art would have clearly recognized that a phase lock loop (PLL) and clock and data recovery (CDR) circuit are generally include a phase detector to generate a voltage signal which represents the difference in phase between two signal input, a charge pump to generate either higher or lower voltage power source for the LPF and VCO using capacitors as storage elements, a low-pass filter (LPF) to attenuate frequencies that are higher than the cutoff frequency, and a voltage controlled oscillator (VCO) to be controlled in oscillation frequency oscillation by a voltage input. To generate the desired voltage power, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a charge pump when designing a (PLL) and (CDR) circuits as taught by Savoj et al. Including a charge pump in the CDR circuit would facilitate the operation of PLL and CDR circuit by providing the higher voltage from a low voltage inputs.

Regarding claim 19:

Izzard et al. further discloses wherein the rate of the quadrature signals of VCO is 1/4 of the received data rate of the phase-error generating circuit **(column 5, lines 31-32)**.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Izzard et al. in view of Savoj et al. as applied to claim 18 and further in view of Laturell et al. and Kocaman et al.

Regarding claim 20:

Izzard et al. and Savoj et al. disclose all of the subject matter as described above except for specifically teaching wherein the phase-error-generating circuit includes: four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals; an error circuit to combine corresponding ones of the latched signals respectively, the error circuit providing a plurality of intermediate signals; and a multiplexing unit to selectively output the intermediate signals as a phase error signal.

However, Laturell et al. in the same field of endeavor teaches latching four latches controllable **(figure 3 clearly shows that the 4 latches 314, 316, 318, and 320 are controllable by the I and Q (quadrature) clock signal)** to latch **(314, 316, 318, and 320 in figure 3)**, at different times according to quadrature clock signals, respectively **(CLK2I, CLK2Q, CLK2IB, AND CLK2QB in figure 3)**, data received by the phase detector **(112 in figures 2 and 3)** so as to form latched signals **(OD1-OD4 in figure 3) (par 0026, lines 7-16, par 0033, lines 1-5, par 0040-par 0048)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Laturell et al. to modify the system and method of Izzard et al. in order to optimize the

clock recovery circuitry by centering the latch function over the time of highest signal level, thereby maximizing signal-to-noise ratio (see par 0008).

Izzard et al., Savoj et al., and Laturell et al. disclose all of the subject matter as described above except for specifically teaching an error circuit to combine corresponding ones of the latched signals respectively, the error circuit providing a plurality of intermediate signals; and a multiplexing unit to selectively output the intermediate signals as a phase error signal.

However, Kocaman et al. in the same field of endeavor, teaches an error circuit **(see four X-OR gates in figure 5)** to combine corresponding ones of the latched signals respectively **(see the latched signals of the four latches in figure 5)**, the error circuit providing a plurality of intermediate signals **(A-D signals output from X-OR gate in figure 5)**; and a multiplexing unit **(decision logic in figure 5)** to selectively output the intermediate signals as a phase error signal **(late/early signal at the output of decision logic unit in figure 5)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use the XOR circuits along with a decision logic unit as taught by Kocaman et al. to modify the system and method of Izzard et al. in order to produce a late/early (phase error) signal (see figure 5).

Allowable Subject Matter

8. Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Kocaman et al. does not teach or suggest the quarter-rate detector further comprises a second set of four latches arranged to receive the outputs of the first set of latches, respectively, and controllable to latch data at different times according to the quadrature clock signals, respectively, so as to form a second set of latched signals; and the second set of four latches representing re-timed versions of the received data.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KABIR A. TIMORY whose telephone number is (571)270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kabir A Timory/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611